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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/938,921	08/24/2001	Walter Clark Milliken	BBNT-P01-128	3501

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EXAMINER	
NGUYEN, QUANG N	
ART UNIT	**PAPER NUMBER**
2141	

DATE MAILED: 09/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/938,921	MILLIKEN ET AL.	
	Examiner	Art Unit	
	Quang N Nguyen	2141	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16 and 18-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16 and 18-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 August 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. *20050614*.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

1. In view of the Appeal Brief filed on 08/04/2005, PROSECUTION IS HEREBY REOPENED. A new ground of rejection is set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) request reinstatement of the appeal.

If reinstatement of the appeal is requested, such request must be accompanied by a supplemental appeal brief, but no new amendments, affidavits (37 CFR 1.130, 1.131 or 1.132) or other evidence are permitted. See 37 CFR 1.193(b)(2).

Claims 1-16 and 18-21 are presented for examination.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-6, 8-13, 16 and 18-21 are rejected under 35 U.S.C. 102(e) as being anticipated by Pandya et al. (US 6,792,502), herein after referred as Pandya.

4. As to claim 1, Pandya teaches a central processing unit (CPU 310 of Figs 7-8), comprising:

an arithmetic logic unit *(ALU 460 as illustrated in Fig. 8);*

a ternary content addressable memory operatively coupled to the arithmetic logic unit within the CPU and configured to perform one or more matching operations *(a CAM 430 coupled to ALU 460 within the CPU 310)* (Pandya, Figs. 7-8 and C11: L14-30).

5. As to claims 2-4, Pandya teaches the CPU of claim 1, wherein the one or more matching operations includes a network packet processing operation, which includes an Internet Protocol (IP) address lookup operation (Pandya, C1:L58 – C2:L3).

6. As to claim 5, Pandya teaches the CPU of claim 1, wherein the one or more matching operations include a packet stuff/unstuff operation (Pandya; C4: L35 - C5:L4).

7. As to claim 6, Pandya teaches the CPU of claim 1, wherein the one or more matching operations include a packet classification operation (Pandya, C3: L10-20).

8. As to claim 8, Pandya teaches the CPU of claim 1, further comprising:

a first register and a second register configured to store a first 32-bit operand and a second 32-bit operand *(since MAC addresses are 48 bits, each MAC address is stored in two consecutive memory entries, i.e., stored in two consecutive 32-bit registers as illustrated in Fig. 5)* (Pandya, Fig. 5 and C9: L22-29).

9. As to claim 9, Pandya teaches the CPU of claim 8, wherein the ternary content addressable memory performs the one or more matching operations based on at least one of the first or second 32-bit operands (Pandya, C9: L33-52).

10. As to claim 10, Pandya teaches the CPU of claim 8, wherein the ternary content addressable memory includes a memory array including a group of 64-bit entries *(inherently, TCAM can be configured for x32, x64, x128 or x256 operations, i.e., N bit operation)*, and wherein, when performing the one or more matching operations, the ternary content addressable memory compares higher order bits of each entry of the memory array to the first 32-bit operand and compares lower order bits of each entry of the memory array to the second 32-bit operand (Pandya, C10: L1-18).

11. As to claim 11, Pandya teaches the CPU of claim 1, wherein the ternary content addressable memory includes a memory array that includes a group of 64-bit entries *(i.e., two consecutive memory entries, i.e., two consecutive 32-bit registers as illustrated in Fig. 5)* (Pandya, Fig. 5 and C9: L22-29).

12. As to claim 12, Pandya teaches the CPU of claim 11, wherein the memory array comprises 32 entries *(i.e., CAM 10 includes a number N of CAM entries or rows 12 where N is any integer greater than zero)* (Pandya, Fig. 1 and C3: L45-49).

13. As to claim 13, Pandya teaches the CPU of claim 1, wherein when performing the one or more matching operations, the ternary content addressable memory is configured to compare an operand to a group of entries *(CAM 10 compares lookup data 32 to all data stored in entries 12)* (Pandya, C4: L35-61).

14. Claims 16, 18-21 are corresponding method and system claims of CPU claims 1, 3 and 6; therefore, they are rejected under the same rationale.

Claim Rejections - 35 USC § 103

15. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

16. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Pandya, in view of J. Robert Lineback ("Virage announces first embedded content-addressable memory for routers, switches"), hereafter referred as Lineback.

17. As to claim 7, Pandya teaches the CPU of claim 1, but does not explicitly teach wherein the ternary content addressable memory is located within the arithmetic logic unit.

In a related art, Lineback teaches on-chip content addressable memories were generated to support hardware-based search engine functions, which are tailored for networking application, such as routers and switches (Lineback, paragraphs [1-3]).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the teachings of Pandya and Lineback to embed the ternary content addressable memory within the arithmetic logic unit to provide support hardware-based search engine functions by quickly examining incoming packets of information and forward them to other systems in the network in a few nanoseconds.

18. Claims 14-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pandya, in view of Nataraj et al. (US 6,757,779), hereafter referred as Nataraj.

19. As to claim 14, Pandya teaches the CPU of claim 13, but does not explicitly teach wherein the ternary content addressable memory is further configured to set a first flag when the operand fails to match an entry in the group of entries, and set a second flag when the operand matches multiple entries of the group of entries.

In a related art, Nataraj teaches the CAM device 1200 may further include logic for generating match flag, multiple flag and/or full-flag signals (Nataraj, C17: L20-22).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the teachings of Pandya and Nataraj to set a first flag when the operand fails to match an entry in the group of entries, and set a second flag when the operand matches multiple entries of the group of entries since such methods were conventionally employed in the art to indicate a match/hit (or multiple match/hit) was found/detected in order to generate an output search result and the address of the matching entry and/of its associated data type are returned.

20. As to claim 15, Pandya-Nataraj teaches the CPU of claim 13, wherein prior to comparing, the ternary content addressable memory is configured to sequentially load the group of entries from a succession of mask/value pairs transferred to the ternary content addressable memory *(the TCAM 404 is configured to sequentially load a group of entries 168.0.0.0/8, 168.69.0.0/16, and 168.69.62.0/24 as illustrated in Fig. 11)* (Nataraj, C16:L47 – C17:L5).

21. Applicant's arguments as well as request for reconsideration filed on 08/04/2005 have been fully considered but they are moot in view of the new ground(s) of rejection.

22. Further references of interest are cited on Form PTO-892, which is an attachment to this office action.

23. A shortened statutory period for reply to this action is set to expire THREE (3) months from the mailing date of this communication. See 37 CFR 1.134.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quang N. Nguyen whose telephone number is (571) 272-3886.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's SPE, Rupal Dharia, can be reached at (571) 272-3880. The fax phone number for the organization is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

RUPAL DHARIA
SUPERVISORY PATENT EXAMINER